UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,730	04/13/2004	Shinobu Nohtomi	XA-10079	2939

181 7590 06/13/2008

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
KARIMI, PEGEMAN	

ART UNIT	PAPER NUMBER
2629	

NOTIFICATION DATE	DELIVERY MODE
06/13/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ipdocketing@milesstockbridge.com
sstiles@milesstockbridge.com

Office Action Summary	Application No.	Applicant(s)	
	10/822,730	NOHTOMI ET AL.	
	Examiner	Art Unit	
	PEGEMAN KARIMI	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22,23,25-28 and 30-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22,23,25-28 and 30-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 04/30/2008 has been entered and considered by the examiner.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Receipt of Japanese Patent Application No. 2003-160538 is acknowledged.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22, 23, 25-28, and 30-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanatani (U.S. Patent No. 5,414,443) in view of Sakaguchi (U.S. Patent No. 7,006,114) and further in view of Lee (U.S. Patent No. 5,905,769).

As to claim 22, Kanatani teaches a method for driving a plurality of pixels (pixels at the intersection of source and gate lines, Fig. 1) in a display panel (100) by a display driver (2) in accordance with a positive phase and a negative phase of a display mode (col. 10, lines 5-7, the method comprising:

inputting display data (Digital Video Signal) to a first driver in the display driver (2);

converting the display data into first display data (first amplitude in Fig. 17(c)) in the positive phase (Vc is in the positive amplitude) and into second display data (second amplitude in Fig. 17(c)) in the negative phase (Vc is in the negative amplitude) using a converting circuit (77, converts the power source into a negative and positive voltage $-V_0 - -V_7$ and $+V_0 - +V_7$) in the display driver (2) in response to a switching signal (79) in synchronization with switching between the positive phase and the negative phase (as can be seen in Fig. 17(a) the voltage is switched between a positive and negative phase and is in synchronization with voltage of counter electrode),

generating a plurality of gradation voltages (col. 12, lines 41-43) using a gradation voltage generating (77) circuit in the display driver (2);

generating (counter electrode drive 8 generates common voltage signals, Fig. 12) a first common voltage in the positive phase (Fig. 17(b) the first amplitude is the first positive voltage) and a second common voltage, different from the first common voltage (the second common voltage is negative , which is different than the first positive common voltage), in the negative phase (Fig. 17(b), the second amplitude is the negative common voltage) using a common voltage driver (8) in the display driver (1), wherein the first and the second common voltage is applied to a common electrode of the plurality of pixels in the display panel (col. 12, lines 58-62);

selecting, using a selector (55) in the display driver (2), a first gradation voltage

($-V_0 - -V_7$, Fig. 17(a)) from the plurality of gradation voltages ($\pm V_0 - \pm V_7$) based on the first display data (first amplitude in Fig. 17(c)) in the positive phase (first amplitude of Vc in Fig. 17(b), which is in the positive phase) and a second gradation voltage ($+V_0 - +V_7$) from the plurality of gradation voltages ($\pm V_0 - \pm V_7$) based on the second display data (second amplitude in Fig. 17(c)) in the negative phase (second amplitude of Vc in fig. 17(b), which is in the negative phase), wherein the first and the second gradation voltages are applied to a pixel electrode (col. 12, lines 48-53) of a selected pixel of the plurality of pixels in the display panel (pixels at the intersection of source and gate lines);

in the positive phase (Fig. 17(b), first positive amplitude of Vc), providing the first gradation voltage (Fig. 17(a), $-V_0 - -V_7$) and the first common voltage (Fig. 17(b), at the interval of $-V_0 - -V_7$, the first common voltage is applied) to the display panel ; and in the negative phase (second amplitude, which is negative phase of Vc), providing the second gradation voltage (Fig. 17(a), $+V_0 - +V_7$) and the second common voltage to the display panel (Fig. 17(b), at the interval of $+V_0 - +V_7$, the second common voltage is applied).

Kanatani does not mention the display data are in the same bit pattern.

Sakaguchi teaches the first display data (Gradation display use data, from 00H-1FH) and the second display data (from 20H-3FH) are in the same bit pattern except for one specified bit (the bits of the gradation display use data are in the same bit pattern, e.g. 00H is in the same bit pattern as 20H, the difference is in MSB) when converting

the display data (37, col. 11, lines 12-15; col. 15, lines 12-19). Therefore it would have been obvious to one of ordinary skilled in the art at the time the invention was made to have added the digital display data for selecting gradation voltage of Sakaguchi to the display device of Kanatani because the display data for selecting gradation voltages of Sakaguchi would provide reduction in power consumption of the driving circuit and miniaturization of a driving circuit (col. 6, lines 1-8 of Sakaguchi).

Kanatani and Sakaguchi do not mention a logic circuit being performed by setting logic "0" and "1" when the switching signal and one specified bit matches or do not matches.

Lee teaches the converting of the display data (202) being performed such that one specified bit of the display data is set to logic "0" by a first exclusive logic circuit (logic zero is produced by an XOR logic circuit if the two inputs match) when the switching signal (e.g. 234-7 can be a switching signal because if the input changes from "1" to "0" the output changes) and the one specified bit (e.g. 234-8) match each other (col. 11, lines 5-7) and

is set to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each other (col. 11, lines 5-7), (XOR logic circuit outputs a logic 1 when the two input values are not equal), and

such that each of other bits of the display data is set to logic "1" by an associated second exclusive logic circuit (XNOR) of a plurality of second exclusive logic circuits (the second group/ bottom group of exclusive logic circuits) when the one specified bit matches the other bit (col. 11, lines 3-5) and set to logic "0" by the associated second

exclusive logic circuit when the one specified bit does not match the other bit (XNOR logic circuit outputs a logic "0" when the two input values are not equal).

Therefore it would have been obvious to one of ordinary skilled in the art at the time the invention was made to have added the logic circuits of Lee to the display driver of Kanatani as modified by Sakaguchi because combining multiple serial signals into a single composite signal, adjusting for any variations in arrival time of each of the serial signals.

As to claim 27, Kanatani teaches a display system (1) comprising:

a display panel (100) including a plurality of signal lines (102), a plurality of scanning lines (101), a common electrode (105), a plurality of pixels coupled to the plurality of signal lines (pixels are at the intersection of the source lines and gate lines and connected to common electrodes), the plurality of scanning lines (gate lines), and the common electrode (105) so that one pixel is coupled to one signal line, one scanning line, and the common electrode (fig. 1, 100),

wherein one pixel includes a MOSFET (104) having a gate coupled to one scanning line (the gate lines is connected to the gate lines 101) and a source-drain path coupled between one signal line and a pixel electrode opposite to the common electrode (source-drain of 104 is connected between the gate line 101 and 103);

a display driver (2) coupled to the plurality of signal lines (102), the plurality of scanning lines (101), and the common electrode (105), wherein the display driver comprises:

a gradation voltage generator (7) providing a plurality of gradation voltages (col. 10, lines 2-7);

a first driver (2) coupled to the plurality of signal lines (102) and including:
a converting circuit (77) coupled to receive display data (circuit 77 is coupled to source driver, which receives signals from a digital video signal) and responsive to a switching signal (79) which controls a switching of a positive phase and a negative phase (col. 11, lines 37-47), and which provides first data (first amplitude in Fig. 17(c)) in the positive phase (Vc is in the positive amplitude) and second data (second amplitude of Fig. 17(c)) in the negative phase (Vc is in the negative amplitude)

selectors (55, $AG_0 - AG_7$) coupled to receive the plurality of gradation voltages ($\pm V_0 - \pm V_7$) and to select ones of the plurality of gradation voltages for the plurality of signal lines (col. 11, lines 37-47), respectively, in response to the first and the second data (first and second amplitude in Fig. 17(c));

a second driver (3) coupled to the plurality of scanning lines (101) and which outputs a selection signal to sequentially select one of the plurality of scanning lines (col. 1, lines 51-52); and
a third driver (8) coupled to the common electrode (105) and which provides, to the common electrode, a first common voltage (e.g. $+V_3 - +V_7$) in the positive phase and which provides, to the common electrode, a second common voltage (e.g. $-V_3 - -V_7$) different from the first common voltage in the negative phase (Fig. 17(a) and (b)), (col. 10, lines 2-15). Kanatani does not mention the display data are in the same bit pattern.

Sakaguchi teaches the first display data (Gradation display use data, from 00H-1FH) and the second display data (from 20H-3FH) are in the same bit pattern except for one specified bit (the bits of the gradation display use data are in the same bit pattern, e.g. 00H is in the same bit pattern as 20H, the difference is in MSB) when converting the display data (37, col. 11, lines 12-15; col. 15, lines 12-19);

Kanatani and Sakaguchi do not mention a logic circuit being performed by setting logic "0" and "1" when the switching signal and one specified bit matches or do not matches.

Lee teaches the converting of the display data (202) being performed such that one specified bit of the display data is set to logic "0" by a first exclusive logic circuit (logic zero is produced by an XOR logic circuit if the two inputs match) when the switching signal (e.g. 234-7 can be a switching signal because if the input changes from "1" to "0" the output changes) and the one specified bit (e.g. 234-8) match each other (col. 11, lines 5-7) and

is set to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each other (col. 11, lines 5-7), (XOR logic circuit outputs a logic 1 when the two input values are not equal), and

such that each of other bits of the display data is set to logic "1" by an associated second exclusive logic circuit (XNOR) of a plurality of second exclusive logic circuits (the second group/ bottom group of exclusive logic circuits) when the one specified bit matches the other bit (col. 11, lines 3-5) and set to logic "0" by the associated second

exclusive logic circuit when the one specified bit does not match the other bit (XNOR logic circuit outputs a logic "0" when the two input values are not equal).

As to Claim 34, this claim differs from claim 27 only in that the limitations "a display driver on a semiconductor substrate" and "a display memory, which stores display data" are additionally recited. The limitation "a display driver on a semiconductor substrate" is well known in the art. Kanatani teaches a display memory (30), which stores display data (col. 8, lines 47-53).

As to claims 23, 28, and 35, Sakaguchi teaches the one specified bit (Most Significant Bit) is the highest order bit (see col. 17, Table 1).

As to claim 25, Kanatani teaches the display driver (2) further comprises a RAM (34), and wherein, in said inputting, the display data is provided from the RAM to the first driver (col. 14, lines 1-3).

As to claim 26, Sakaguchi teaches wherein, in said inputting, the display data is provided from a microcomputer (4), (col. 8, lines 32-33).

As to claim 30, Kanatani teaches the display driver (2) further comprises a display memory (34) which provides the display data (col. 14, lines 1-3).

As to claims 31 and 32, the limitation "the display driver is on a semiconductor substrate" is well known in the art.

As to claim 33, Sakaguchi teaches a microcomputer (4) which provides the display data (col. 8, lines 32-33).

Response to Arguments

5. Applicant's arguments with respect to claims 22, 23, 25-28, and 30-35 have been considered but are moot in view of the new ground(s) of rejection.

The reference of Lee (U.S. Patent No. 5,905,769) has been added for the new ground of rejection.

The amended claims mention an exclusive logic circuit, which setting one specified bit of the display data to logic "0" when the switching signal and the one specified bit match each other. This is the description of an exclusive-OR (XOR) circuit.

Also a second exclusive logic circuit, which setting other bits to logic "1" when the one specified bit matches the other bit. This is the description of an exclusive-NOR (XNOR) circuit.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boudon (U.S. Pub. No. 2004/0123004) teaches an XOR circuit and how the circuit operates.

Barkans (U.S. Patent No. 5,905,504) teaches a system having XNOR and XOR circuits for dithering and quantizing image data to optimize visual quality of a color recovered image.

Inquiry

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PEGEMAN KARIMI whose telephone number is (571)270-1712 and direct fax number is (571) 270-2712. The examiner can normally be reached on Monday-Thursday 8:00am - 5:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen can be reached on (571) 272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Pegeman Karimi/
Examiner, Art Unit 2629
June 5, 2008

/Chanh Nguyen/
Supervisory Patent Examiner, Art Unit 2629